MULTI CCD ELECTRONICS
for ground and space applications

Orbital AEROSPACE SYSTEMS

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ABSTRACT

Orbital Aerospace has developed a front-end electronics that commands independently two space spectrometers which focal planes are base on a CCD from e2v manufacturer. The product developed is highly flexible and configurable and it has been designed to support different families of e2v products including NIMO and AIMO devices, performing benchmarking of the product and exploring the devices characteristics beyond their limits together with e2v. The key features are low noise, reliable, high speed and space radiation compensation. Based on a flexible FPGA Core from Orbital this product is easily adaptable to multiple needs and requirements and ready to be used in astronomical instruments.

HIGH SPEED

The CCD readout speed is software configurable in order to conform to the requirements of the application.
Through improved clock mechanisms (adjustable overlay "image clock"), can be obtained transfer line rates of 100 kHz.

Fig.1 - The image shows a reading of a CCD with a good CTE (left) compared to one that has been degraded (right)

High configurable system lets to characterize devices, with the aim of obtain transfer rates in ensuring a CTE value (Charge Transfer Efficiency).).

SELECTABLE REGION OF INTEREST (ROI)

There are applications that do not require the full use of the entire region of the CCD. Through the selection of the ROI you can optimize the reading of the area illuminated by the optic.
This feature allows obtain frame-transfer characteristics in a full-frame CCD.

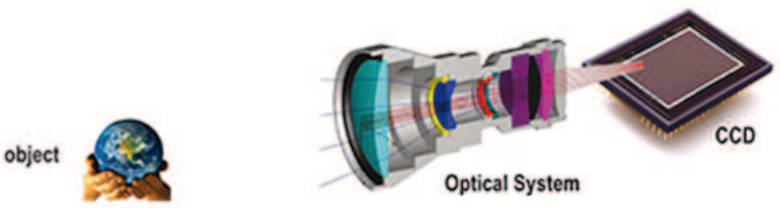


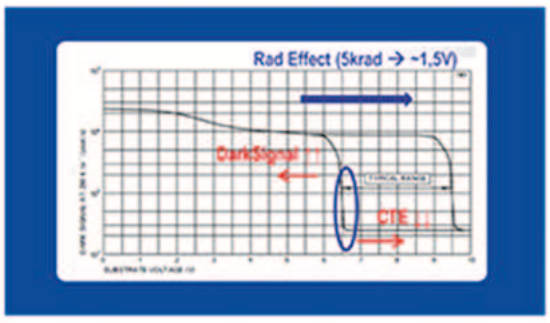
Fig. 2 - The optics illuminate only a part of the device. Why read all of the CCD?

Binning Mode - Binning is the addition of signal charge from more than one pixel into a given location. It may be performed in either horizontal or vertical directions by performing the summation onto the output node.

Cleanup Mode - is possible to perform cleaning of the CCD charge with the purpose of minimize noise and dark current.

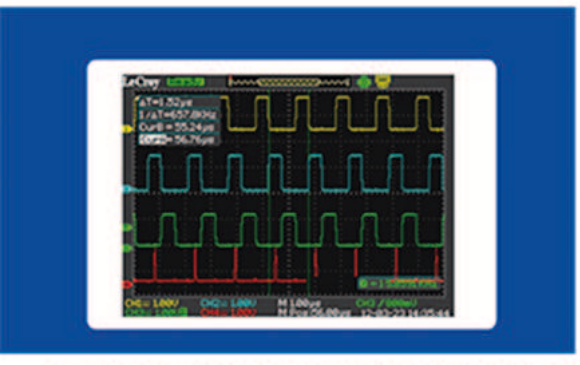
SPACE RADIATION COMPENSATION

One of the results from ionising radiation is to increase surface dark signal, so operation with Vss in a condition to pin the silicon under low clocks is essential to suppress this increase. The other main result is to generate fixed charge in the gate dielectric. This acts as a fixed bias shift in the direction that needs Vss to be increased to maintain pinning. During flight, due to ionising radiation, Vss will be progressively reduced. For example, 10kRads result is a change threshold ~ 2 V, which has the effect of reducing Vss by 2V.
Shift the voltage of the substrate can obtain a compensation of the effects of radiation. The system is designed with several discrete values between the Vss and Vss+2V (10krad effect) in order to compensate the radiation effect on board. This value it can change by software when the system requires the change.



Graph 1 - Substrate Voltage vs Dark Signal vs Rad Effect
The voltage of the substrate (Vss) must be set between the values that reduce dark current and can achieve good load transfer between lines. Radiation shifts this optimum value of Vss, making it necessary to change this value in flight.

OUTPUT NOISE REDUCED



The CCD output register can be read at a speed configurable according to noise levels and application, obtaining a maximum value of 2MHz. The design has been made by selecting low noise electronic components

Via a system of "Clamp & Sample" configurable opens the range to read whatever record of CCD, always offering sampling at the optimum time.

Fig.3 - The read phases of CCD (R's) with a configurable Clamp signal. It can clamp the output value in the optimal instant of charge.

FEATURES

Highly configurable

FPGA based.
SW configurable parameters.
Selectable ROI.
Cleanup and binning modes.
IP library with extra functionality.

High performance

Fast image transfer and readout register.
Advanced methodologies to improve CTE.
Minimized Dark Signal & Noise
Radiation Compensation
SoC with Leon Architecture.

Simple design integration

Support plug&play capabilities on APB bus.
Commercial grade.
Easily grow up to space system.

FRONT END ELECTRONICS

FPGA Based

Synthesizable hardware design in FPGA's provides numerous appealing choices for the design of SoC (System On Chip) needed in the development of technology in the space environment.

The IP-Core developed by Orbital is designed to be replicated and reused as needed by the project.
The gate of the CCDs arrays opens with multiple IP-Core instantiations within the same FPGA and controlled by the same bus.

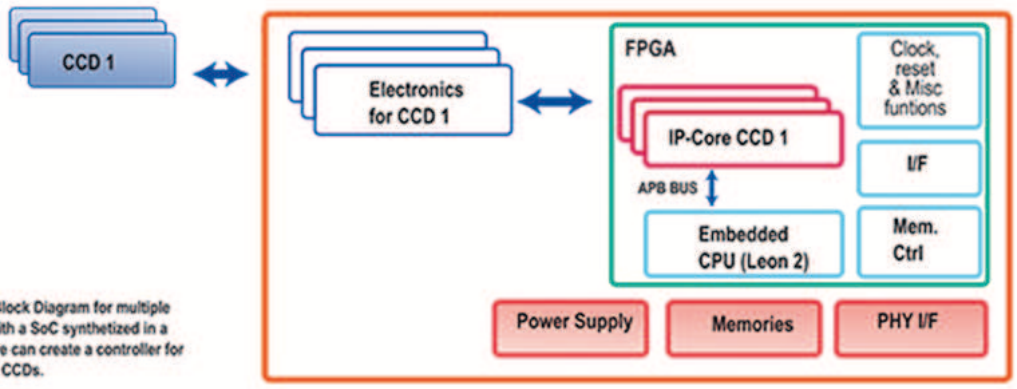


Fig 4 - Block Diagram for multiple CCD. With a SoC synthetized in a FPGA we can create a controller for array of CCDs.

Using IP-Cores Orbital property provides added functionality to the system, such as communications interfaces, mass storage systems with DMA, corrector errors.

Plug & Play

AMBA APB interface that allows "plug and play" systems Leon architecture-based. Configurable parameters are mapped in the APB registers. The CCD controller is plugged as a slave.

Mass storage system data on memories using DMA allows the CPU execute control tasks during CCD readout periods.

Addr Offset	Usage
0x00	Control Signals
0x08	Integration Time
0x10	Binning Mode
0x18	Cleanup Mode
0x20	ROI
0x28	Freq. I's
0x30	Freq. R's
0x38	Mem Ctrl
0x40	Count Frames
0x48	Err. Ctrl

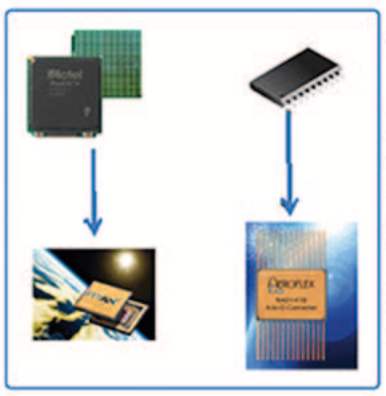
Table 1. Shown the basic configuration registers on APB Bus.

Commercial Grade

Complete system of supply, digitizing and signal adaptation with commercial and industrial grade components. Ideal for labs and study of new devices.

The hardware solution is highly configurable. The gain of the digitization system is configurable and the band pass filter could fix in the operation frequency in order to minimize the noise.

The reprogrammable flash technology and the high capacity of the FPGA give to the system flexibility. Furthermore, the Aldec adapter with an Actel device offer the same pinout of a RTAX for the easily grow up to space application.



Space grade

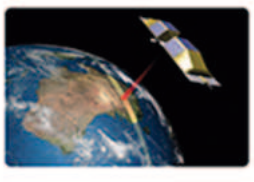
Design equivalent to commercial with space grade components. The space design is centered in the RTAX -2000 offer industry-leading advantages as hight performance, low-power consumption, great capacity in a SEU hardened FPGA.

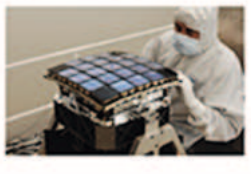
APPLICATIONS


Characterize and study new devices on laboratory

Astronomic Applications

Space Applications





CCD Array

Spectroscopy